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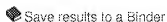
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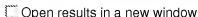


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1 [Hardware-software trade-offs in a direct Rambus implementation of the](#)[RAMpage memory hierarchy](#)

Philip Machanick, Pierre Salverda, Lance Pompe

December 1998 ACM SIGOPS Operating Systems Review, Volume 32 Issue 5

Publisher: ACM

Full text available: pdf(1.47 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

The RAMpage memory hierarchy is an alternative to the traditional division between cache and main memory: main memory is moved up a level and DRAM is used as a paging device. The idea behind RAMpage is to reduce hardware complexity, if at the cost of ...

2 [Lightweight Implementation of the POSIX Threads API for an On-Chip MIPS Multiprocessor with VCI Interconnect](#)

Frederic Petrot, Pascal Gomez

March 2003 DATE '03: Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2, Volume 2

Publisher: IEEE Computer Society

Full text available: pdf(132.65 KB) [Publisher Site](#)Additional Information: [full citation](#),
[abstract](#),  
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This paper relates our experience in designing from scratch a multi-threaded kernel for a MIPS R3000 on-chip multiprocessor. We briefly present the target architecture build around a VCI compliant interconnect, and the CPU characteristics. Then we focus ...

3 [Robust wait-free hierarchies](#)

Prasad Jayanti

July 1997 Journal of the ACM (JACM), Volume 44 Issue 4

Publisher: ACM

Full text available: pdf(362.27 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

The problem of implementing a shared object of one type from shared objects of other types has been extensively researched. Recent focus has mostly been on wait-free implementations, which permit every process to complete its operations ...

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Keywords: MIMD, asynchronous computing, hierarchy, implementation, robustness, shared memory, shared objects, synchronization, wait-freedom

#### 4 [Adaptive two-level thread management for fast MPI execution on shared memory machines](#)

Kai Shen, Hong Tang, Tao Yang

January 1999 Supercomputing '99: Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM)

Publisher: ACM

Full text available:  pdf(152.63 KB)

Additional Information: full citation, references, cited by, index terms

#### 5 [Energy-aware lossless data compression](#)

Kenneth C. Barr, Krste Asanović

August 2006 ACM Transactions on Computer Systems (TOCS), Volume 24 Issue 3

Publisher: ACM

Full text available:  pdf(673.90 KB)

Additional Information: full citation, abstract, references, index terms

Wireless transmission of a single bit can require over 1000 times more energy than a single computation. It can therefore be beneficial to perform additional computation to reduce the number of bits transmitted. If the energy required to compress data ...

Keywords: Compression, energy-aware, lossless, low-power, power-aware

#### 6 [A portable thread API for teaching operating systems](#)

Jeffrey D. Martens

June 2003 Journal of Computing Sciences in Colleges, Volume 18 Issue 6  
Publisher: Consortium for Computing Sciences in Colleges

Full text available:  pdf(40.40 KB)

Additional Information: full citation, abstract, references, index terms

When teaching a course that includes programming assignments, it can be expedient to allow students a choice in programming language and operating systems, e.g. Java or C++, Windows or Linux, etc. In addition to saving classroom time, this allows the ...

#### 7 [A scalable approach to thread-level speculation](#)

J. Gregory Steffan, Christopher B. Colohan, Antonia Zhai, Todd C. Mowry

June 2000 ISCA '00: Proceedings of the 27th annual international symposium on Computer architecture

Publisher: ACM

Full text available:  pdf(186.97 KB)

Additional Information: full citation, abstract, references, cited by, index terms

While architects understand how to build cost-effective parallel machines across a wide spectrum of machine sizes (ranging from within a single chip to large-scale servers), the real challenge is how to easily create parallel software ...

8 [Data-centric security, role analysis and role tpestates](#)

Vugranam C. Sreedhar

June 2006 SACMAT '06: Proceedings of the eleventh ACM symposium on Access control models and technologies

Publisher: ACM

Full text available: [pdf\(270.88 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In J2EE and .NET roles are assigned to methods using external configuration files, called the deployment descriptors. Assigning roles to methods, although conceptually simple, in practice it is quite complicated. For instance, in order for a deployer ...

Keywords: RBAC, role analysis, role escape analysis, role tpestates

9 [Automatic data movement and computation mapping for multi-level parallel architectures with explicitly managed memories](#)

Muthu Manikandan Baskaran, Uday Bondhugula, Sriram Krishnamoorthy, J. Ramanujam, Atanas Rountev, P. Sadayappan

February 2008 PPoPP '08: Proceedings of the 13th ACM SIGPLAN Symposium on Principles and practice of parallel programming

Publisher: ACM

Full text available: [pdf\(235.81 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Several parallel architectures such as GPUs and the Cell processor have fast explicitly managed on-chip memories, in addition to slow off-chip memory. They also have very high computational power with multiple levels of parallelism. A significant challenge ...

Keywords: data movement, graphics processor unit, multi-level tiling, scratchpad memory

10 [Tradeoff between data-, instruction-, and thread-level parallelism in stream processors](#)

Jung Ho Ahn, Mattan Erez, William J. Dally

June 2007 ICS '07: Proceedings of the 21st annual international conference on Supercomputing

Publisher: ACM

Full text available: [pdf\(410.51 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper explores the scalability of the Stream Processor architecture along the instruction-, data-, and thread-level parallelism dimensions. We develop detailed VLSI-cost and processor-performance models for a multi-threaded Stream Processor and ...

Keywords: DLP, ILP, TLP, aspect ratio, stream processors

11 [Mining evolution data of a product family](#)

Michael Fischer, Johann Oberleitner, Jacek Ratzinger, Harald Gall

May 2005 MSR '05: Proceedings of the 2005 international workshop on Mining software repositories

Publisher: ACM


Full text available: [pdf\(254.59 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Diversification of software assets through changing requirements impose a constant challenge on the developers and maintainers of large software

systems. Recent research has addressed the mining for data in software repositories of single products ranging ...

## 12 Data protection and data sharing in telematics

Sastry Duri, Jeffrey Elliott, Marco Gruteser, Xuan Liu, Paul Moskowitz, Ronald Perez, Moninder Singh, Jung-Mu Tang  
December 2004 Mobile Networks and Applications, Volume 9 Issue 6  
Publisher: Kluwer Academic Publishers


Full text available:  pdf(303.67 KB) Additional Information: full citation, abstract, references, cited by, index terms

Automotive telematics may be defined as the information-intensive applications enabled for vehicles by a combination of telecommunications and computing technology. Telematics by its nature requires the capture, storage, and exchange of sensor data to ...

Keywords: automotive telematics, data protection architecture, privacy policies

## 13 Efficient software implementation of embedded communication protocol controllers using asynchronous software thread integration with time- and space-efficient procedure calls

Nagendra J. Kumar, Vasanth Asokan, Siddhartha Shivshankar, Alexander G. Dean  
February 2007 ACM Transactions on Embedded Computing Systems (TECS), Volume 6 Issue 1  
Publisher: ACM


Full text available:  pdf(586.75 KB) Additional Information: full citation, abstract, references, index terms

The overhead of context switching limits efficient scheduling of multiple concurrent threads on a uniprocessor when real-time requirements exist. A software-implemented protocol controller may be crippled by this problem. The available idle time may ...

Keywords: Asynchronous software thread integration, J1850, fine-grain concurrency, hardware to software migration, software-implemented communication protocol controllers

## 14 Memory-efficient and thread-safe quasi-destructive graph unification

Marcel P. van Lohuizen  
October 2000 ACL '00: Proceedings of the 38th Annual Meeting on Association for Computational Linguistics  
Publisher: Association for Computational Linguistics


Full text available:  pdf(249.98 KB) Additional Information: full citation, abstract, references, cited by

In terms of both speed and memory consumption, graph unification remains the most expensive component of unification-based grammar parsing. We present a technique to reduce the memory usage of unification algorithms considerably, without increasing execution ...

## 15 A "flight data recorder" for enabling full-system multiprocessor deterministic replay

Min Xu, Rastislav Bodik, Mark D. Hill  
May 2003 ACM SIGARCH Computer Architecture News, Volume 31 Issue 2

Publisher: ACM

Full text available:  pdf(311.95 KB) Additional Information: full citation, abstract, references, cited by

Debuggers have been proven indispensable in improving software reliability. Unfortunately, on most real-life software, debuggers fail to deliver their most essential feature --- a faithful replay of the execution. The reason is non-determinism caused ...

#### 16 Easing the management of data-parallel systems via adaptation



David Petrou, Khalil Amiri, Gregory R. Ganger, Garth A. Gibson  
September 2000 EW '9: Proceedings of the 9th workshop on ACM SIGOPS European workshop: beyond the PC: new challenges for the operating system

Publisher: ACM

Full text available:  pdf(146.51 KB) Additional Information: full citation, abstract, references


In recent years we have seen an enormous growth in the size and prevalence of data processing workloads [Fayyad 1998, Gray 1997]. The picture that is becoming increasingly common is depicted in Figure 1. In it, organizations or resourceful individuals ...

#### 17 Shared-stack cooperative threads



Boncheol Gu, Yongtae Kim, Junyoung Heo, Yookun Cho  
March 2007 SAC '07: Proceedings of the 2007 ACM symposium on Applied computing

Publisher: ACM

Full text available:  pdf(228.87 KB) Additional Information: full citation, abstract, references, index terms

Multithreaded sensor operating systems provide the paradigm of threads which enables programmers to program and maintain their applications more easily. However, a lot of memory space can be wasted due to the fact that a fixed-size stack is allocated ...


Keywords: cooperative task management, multithread system, operating systems, sensor operating systems, shared-stack

#### 18 Dynamic hot data stream prefetching for general-purpose programs



Trishul M. Chilimbi, Martin Hirzel  
June 2002 PLDI '02: Proceedings of the ACM SIGPLAN 2002 Conference on Programming language design and implementation

Publisher: ACM

Full text available:  pdf(219.85 KB) Additional Information: full citation, abstract, references, cited by, index terms

Prefetching data ahead of use has the potential to tolerate the growing processor-memory performance gap by overlapping long latency memory accesses with useful computation. While sophisticated prefetching techniques have been automated for limited ...


Keywords: data reference profiling, dynamic optimization, dynamic profiling, memory performance optimization, prefetching, temporal profiling

#### 19 Data dissemination techniques for distributed simulation environments

Bryan Horling, Victor Lesser

December 2004 WSC '04: Proceedings of the 36th conference on Winter simulation

Publisher: Winter Simulation Conference

Full text available:  pdf(212.83 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

Farm is a distributed simulation environment for modeling the performance of large-scale multi-agent systems. It uses a component-based architecture to distribute the computational load of the simulation and improve running time. It also supports a global ...


## 20 [Function level parallelism driven by data dependencies](#)



Sean Rul, Hans Vandierendonck, Koen De Bosschere

March 2007 ACM SIGARCH Computer Architecture News, Volume 35 Issue 1

Publisher: ACM





Full text available:  pdf(1.35 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

With the rise of Chip multiprocessors (CMPs), the amount of parallel computing power will increase significantly in the near future. However, most programs are sequential in nature and have not been explicitly parallelized, so they cannot exploit these ...

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